**Implementation of an Efficient Multiplier based on *Urdhva Tiryakbhyam Sutra***

**ABSTRACT**

A high speed processor depends greatly on the multiplier as it is one of the key hardware blocks in most digital signal processing systems as well as in general processors. This paper presents a high speed 8x8 bit Vedic multiplier architecture which is quite different from the Conventional method of multiplication like add and shift. The most significant aspect of the proposed method is that, the developed multiplier architecture is based on Vertical and Crosswise structure of Ancient Indian Vedic Mathematics. It generates all partial products and their sum in one step. This also gives chances for modular design where smaller block can be used to design the bigger one. So the design complexity gets reduced for inputs of larger no of bits and modularity gets increased. The proposed Vedic multiplier is coded in VHDL (Very High Speed Integrated Circuits Hardware Description Language), synthesized and simulated using EDA (Electronic Design Automation) tool - XilinxISE12.1i. Finally the results are compared with Conventional multipliers to show the significant improvement in its efficiency in terms of path delay (speed). The high speed processor requires high speed multipliers and the Vedic Multiplication technique is very much suitable for this purpose***.***

**LANGUAGE USED:**

**TOOLS REQUIRED:**

* MODELSIM – Simulation
* XILINX-ISE – Synthesis